FEDERAL PUBLIC SERVICE COMMISSION
COMPETITIVE EXAMINATION-2025 FOR RECRUITMENT TO POSTS IN BS-17 UNDER THE FEDERAL GOVERNMENT
COMPUTER SCIENCE, PAPER-II

Roll Number

TIME ALLOWED: THREE HOURS	**(PART-I MCQs)**	**MAXIMUM MARKS: 20**
PART-I (MCQs) : MAXIMUM 30 MINUTES	**(PART-II)**	**MAXIMUM MARKS: 80**

NOTE: (i) First attempt **PART-I (MCQs)** on separate **OMR Answer Sheet** which shall be taken back after **30 minutes.**
(ii) Overwriting/cutting of the options/answers will not be given credit.
(iii) There is **no negative** marking. All MCQs must be attempted.

PART-I (MCQs)(COMPULSORY)

Q.1. (i) Select the best option/answer and fill in the appropriate Box ☐ on the **OMR Answer Sheet.(20x1=20)**
(ii) Answers given anywhere else, other than OMR Answer Sheet, will not be considered.

1. **A stack is:**
   (A) An 8 bit register in microprocessor (B) A 16 bit register in microprocessor
   (C) A set of memory location in R/WM reserved for storing information temporarily during the execution of computer. (D) A 16-bit memory address stored in program counter
2. **Data hazards occur when:**
   (A) Greater performance loss (B) Pipeline changes the order of read/write access to operands
   (C) Some functional unit is not fully pipelined (D) Machine size is limited
3. **If computer A executes a program in 10 seconds & Computer B runs same in 15 seconds, how much faster is computer A than B?**
   (A) 5.1 times (B) 1.4 times (C) 1 time (D) 1.5 times
4. **Processor having Clock cycle of 0.25ns will have clock rate of:**
   (A) 2 GHz (B) 3 GHz (C) 4 GHz (D) 8 GHz
5. **Which of the following comes under the application of image blurring?**
   (A) Object detection (B) Gross representation (C) Object motion (D) Image segmentation
6. **For a continuous image f(x, y), Quantization is defined as:**
   (A) Digitizing the coordinate values (B) Digitizing the amplitude values
   (C) Both (A) & (B) (D) None of these
7. **What is the method that is used to generate a processed image that has a specified histogram?**
   (A) Histogram linearization (B) Histogram equalization
   (C) Histogram matching (D) Histogram processing
8. **A _____ in a table represents a relationship among a set of values.**
   (A) Column (B) Key (C) Row (D) Entry
9. **Which forms are based on the concept of functional dependency?**
   (A) 1NF (B) 2NF (C) 3NF (D) 4NF
10. **In case of any shutdown during transaction before commit, which of the following statement is done automatically?**
    (A) View (B) Commit (C) Rollback (D) Flashback
11. **Process synchronization can be done on:**
    (A) Hardware level (B) Software level (C) Both (A) & (B) (D) None of these
12. **Which module gives control of the CPU to the process selected by the short-term scheduler?**
    (A) Dispatcher (B) Interrupt (C) Scheduler (D) None of these
13. **If the semaphore value is negative:**
    (A) Its magnitude is the number of processes waiting on that semaphore (B) It is invalid
    (C) No operation can be further performed on it until the signal operation is performed on it
    (D) None of these
14. **For 3 page frames, the following is the reference string:**
    7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1
    How many page faults does the LRU page replacement algorithm produce?
    (A) 10 (B) 15 (C) 11 (D) 12
15. **What is DOM?**
    (A) Hierarchy of objects in ASP.NET (B) Application programming interface
    (C) Convention for representing and interacting with objects in html documents
    (D) Language dependent application programming

16. **Which error is invoked when SQLTransaction Callback does not execute?**
    (A) INVALID_ACCESS_ERR (B) UNKNOWN_ERR
    (C) TIMEOUT_ERR (D) INVALID_STATE_ERR
17. **Which of the following property defines labels for a list of items?**
    (A) List-shape (B) List-style (C) List-type (D) List-style-type
18. **ICMP is primarily used for:**
    (A) Error and diagnostic functions (B) Addressing (C) Forwarding (D) Routing
19. **Which multiplexing technique is used to transmit digital signals?**
    (A) FDM (B) TDM (C) WDM (D) FDM & WDM
20. **DHCP (dynamic host configuration protocol) provides _____ to the client.**
    (A) IP address (B) MAC address (C) Url (D) None of these

PART – II

NOTE: (i) **Part-II** is to be attempted on the separate **Answer Book.**
(ii) Attempt **ONLY FOUR** questions from **PART-II** by selecting **TWO** questions from **EACH SECTION**. **ALL** questions carry **EQUAL** marks.
(iii) All the parts (if any) of each Question must be attempted at one place instead of at different places.
(iv) Candidate must write Q. No. in the Answer Book in accordance with Q. No. in the Q.Paper.
(v) No Page/Space be left blank between the answers. All the blank pages of Answer Book must be crossed.
(vi) Extra attempt of any question or any part of the attempted question will not be considered.

(SECTION – A)

Q. No. 2. **(a)** An instruction requires five stages to execute: **(3)**

Stage-1 (instruction fetch) requires	=	30 ns
Stage-2 (instruction decode)	=	9 ns
Stage-3 (instruction execute)	=	20 ns
Stage-4 (Memory access)	=	35 ns
Stage-5 (Store results)	=	10 ns

An instruction must proceed through the stages in sequence. What is the minimum asynchronous time for any single instruction to complete?

(b) Consider a single-level cache with an access time of 2.5 ns, a line size of 64 bytes, and a hit ratio of H = 0.95. Main memory uses a block transfer capability that has a firstword (4 bytes) access time of 50 ns and an access time of 5 ns for each word thereafter.

(i) What is the access time when there is a cache miss? Assume that the cache waits until the line has been fetched from main memory and then re-executes for a hit. **(3)**

(ii) Suppose that increasing the line size to 128 bytes increases the H to 0.97. Does this reduce the average memory access time? **(4)**

(c) **(i)** Compare the set of addressing modes of RISC and CISC machines. Give one example of addressing modes used in RISC and CISC respectively. **(5)**

(ii) Explain Parallel Processing, and also draw pipeline processing for instruction: Ai*Bi+Ci **(5)**

Q. No. 3. **(a)** **Answer the Following Questions:**

(i) Is it possible for an organization's Web server and mail server to have exactly the same alias for a hostname (for example, foo.com)? What would be the type for the RR that contains the hostname of the mail server? **(2)**

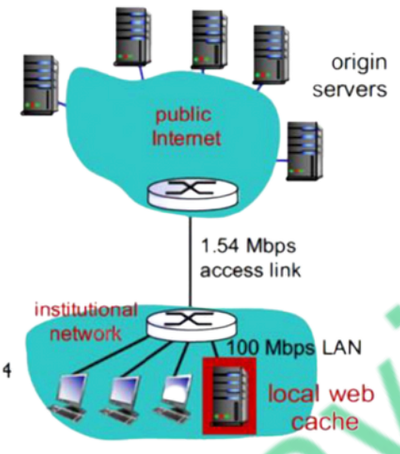
(ii) Draw the structure of Internet in terms of ISPs, also show the concept in terms of Edge and Core networks. **(3)**

(iii) A packet switch receives a packet to be forwarded. When the packet arrives, one other packet is halfway done being transmitted on this outbound link and four other packets are waiting to be transmitted in FIFO manner. Suppose all packets are 1,500 bytes and the link rate is 2 Mbps. What is the queuing delay for the packet? **(3)**

(iv) Why do HTTP, FTP, SMTP, and POP3 run on top of TCP rather than on UDP? **(2)**

(b) **(i)** Why do we need conditional GET when we have regular GET with respect to HTTP? What is its difference in comparison to GET? **(4)**

(ii) With respect to web caching, if an average object size is 100K bits and the average request rate from browsers to origin servers is 15/sec. Suppose RTT from an institutional router to any origin server is 2 sec. If LAN speed is 100Mbps and access link speed is 1.54 Mbps then with a cache hit of 50%, how much total delay will be there? **(6)**



Q. No. 4. **(a)** A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count: **(10)**

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

(b) What are the differences among sequential access, direct access, and random access? Also, write and explain the general relationship among access time, memory cost, and capacity. **(10)**

Q. No. 5. **(a)** Consider the following pseudo code for producer and consumer:

// producerdo{	// consumerdo{
//produce an item	// remove item from buffer
//place in buffer	// consumes item
}while(true);	}while(true);

(i) What is race condition? **(2)**

(ii) Is there any possibility of the race condition if two threads named producer and consumer simultaneously execute the above functions? Provide the reasoning in two-three sentences. **(2)**

(iii) Add the necessary synchronization in the above functions, you may use semaphores or mutex. You may provide just pseudo code or exact C/C++ code. **(3)**

(iv) Consider a process that uses a user level threading library to spawn 10 user level threads. The library maps these 10 threads on to 2 kernel threads. The process is executing on a 8-core system. What is the maximum number of threads of a process that can be executing in parallel? **(3)**

(b) Consider a multi-level memory management scheme with the following format for virtual addresses:

Virtual Page # (10 bits)	Virtual Page # (10 bits)	Offset (12 bits)

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Virtual addresses are translated into physical addresses of the following form:

Physical Page # (20 bits)	Offset (12 bits)

Page table entries (PTE) are 32 bits and contain the 20-bit physical page number and OS bookkeeping bits (e.g., valid, dirty, used, etc.).

(i) How big is a page? **(1)**

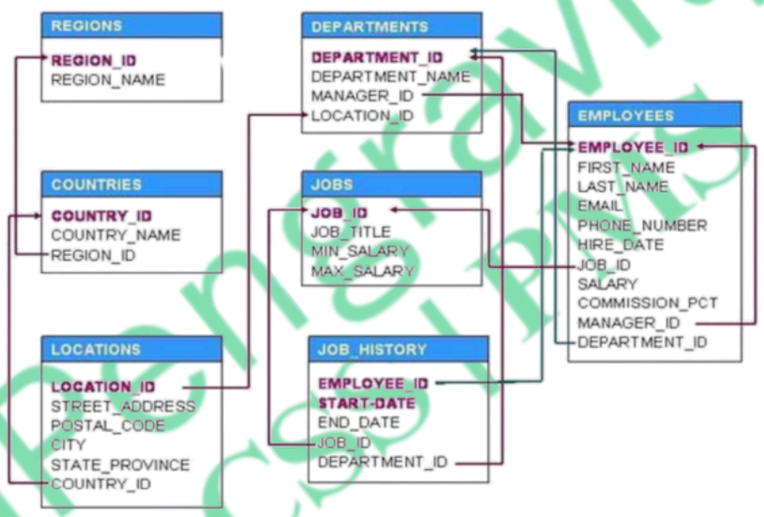
(ii) What is the maximum amount of memory (in bytes) in a single virtual address space? Explain your answer. **(3)**

(iii) What is the maximum amount of physical memory (in bytes) that this memory management scheme supports? Explain your answer. **(3)**

(iv) Sketch the format of the page table for the multi-level virtual memory management scheme. Illustrate the process of resolving an address as well as possible. Assume there is no TLB or cache. **(3)**

(SECTION – B)

Q. No. 6. **(a)** Answer the questions i, ii, according to given schema.



(i) Display the length of first name and length of second name for employees where last name contains character 'b' after 3rd position. **(2)**

(ii) Display job title, department name, employee last name, starting date for all jobs from 1992 to 1998. **(3)**

(iii) Differentiate between Left outer join, Right outer join and Full outer join. Explain your answer with the help of Venn Diagram. **(5)**

(b) Provide brief answers to the following questions:

(i) Differentiate between Single row Sub-Query and Multi row Sub-Query and write a sample query too. **(5)**

(ii) Discuss the role of Primary Keys, foreign keys, and indexes in database schema. Also, explain their significance in ensuring data accuracy, enforcing referential integrity and improving query performance. **(5)**

Q. No. 7. **(a)** In the context of compression, differentiate between coding, spatial and temporal redundancies. **(6)**

(b) What is translation and scaling? Find the number of bits required to store a 256x256 image with 32 gray levels. **(6)**

(c) What is Histogram equalization? Explain the process and discuss its uses. **(8)**

Q. No. 8. **(a)** What is the role of requirement engineering in web engineering? List functional and non- functional requirements for a website. **(6)**

(b) What are different security mechanisms used for encrypting the contents of a website? Explain any one in detail. **(6)**

(c) Explain 3-tier web application architecture. **(8)**

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